

IST-055
Development of Ultra-fast DSP Algorithms for Agile Parallel Computers

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Abstract

Recent research at GateChange Technologies has led to the development of VLSI chips containing up to 257 independent processors with their own memories embedded in a communication fabric. This communication fabric allows fast and transparent setting up of multiple random communication channels to do the inter-processor data movement. Since the communication channels are made and broken at will, these parallel computers exhibit little or no communication bottlenecks.

This project aims at developing fast structured algorithms suitable for parallel architectures with such agile interconnection networks. It focuses on the computations of discrete Fourier and discrete Cosine transforms. Our algorithm development uses group theoretic foundations and results in very efficient bilinear algorithms. The regular structure of the final algorithms allows proper distribution in a multiprocessor architecture, thereby ensuring extremely fast computation. Our preliminary results on bilinear algorithms for discrete Fourier transforms of length 2^n show that the proposed methods are feasible and provide a speed-up of $O(n)$ over the best known algorithms.