IST-048
High-Performance VLSI Architectures for Iterative Decoders

Zhiyuan Yan
Assistant Professor, Department of Electrical and Computer Engineering, Lehigh University, Bethlehem, PA

Maximilien Gadouleau
Graduate Student, Department of Electrical and Computer Engineering, Lehigh University, Bethlehem, PA

Industry Participants
GateChange Technologies, Inc.

Abstract
The project targeted by this proposal is the first phase of a two-phase research plan, and it is critical in realizing the long-term goals. Specifically, this project will study and evaluate the iterative decoding algorithms in the context of VLSI implementation, devise new decoding algorithms that are suitable for VLSI implementation. In Phase II of our research plan, the new decoding algorithms will be fully implemented and performances will be evaluated. Hence, the new algorithms tailored to VLSI implementation are the bridge between the two phases, and play a vital part in the whole research plan.