Abstract
Error-correcting codes are utilized to protect reliable transmission of information against possible corruptions in virtually all communication and data storage systems. The recently proposed error-correcting codes defined on graphs promise excellent performances in theory, but in practice few applications can utilize these codes due to the difficulty in implementing the iterative decoders for these codes in very-large-scale integration (VLSI). The PI and his graduate students aim to address this key issue and design high-performance VLSI architectures for iterative decoders by using a jointly algorithmic and architectural approach. This research effort consists of two phases, and the project targeted by this proposal is the second phase, during which new VLSI architectures for iterative decoders will be devised and implemented. Successful completion of this research endeavor will alleviate the difficulty in the VLSI implementation of the iterative decoders, and will pave the way for more widely applications of the codes on graphs.

Due to the ubiquitous utilization of the error-correcting codes, this project has broad technical and economical impacts since our research results will spawn new technologies in a wide range of areas and will allow various industries to turn the superb performances of the codes on graphs into better products. Our research efforts have educational impacts as well: the research activities in this project will improve the skills of Pennsylvania’s future work force by providing industry experience to the participating graduate students and by incorporating the obtained results in new courses at Lehigh University.